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/William R. Allen/ January 8, 2007
William R. Allen Date

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Furukawa et al. | Art Unit: | 2814 |
| Serial No.: | 10/767,039 | Examiner: | Phat X. Cao |
| Filed: | January 29, 2004 | Atty. Docket No.: | ROC920030272US1 |
| For: | VERTICAL FIELD EFFECT TRANSISTORS INCORPORATING SEMICONDUCTING NANOTUBES GROWN IN A SPACER-DEFINED PASSAGE | | |

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## COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants' undersigned counsel notes the Examiner's Statement of Reasons for Allowance attached with the Notice of Allowability. The reasons set forth by the Examiner refer only to some of the features in independent claims 1, 42, and 47, and are not the only reasons that all of the claims are allowable.

With respect to independent claim 1, the prior art fails to disclose or suggest a vertical semiconductor device structure, comprising: a substrate defining a substantially horizontal plane; a gate electrode projecting vertically from said substrate and including a vertical sidewall; a semiconducting nanotube extending between opposite first and second ends with a substantially vertical orientation; a spacer of a dielectric material flanking said vertical

sidewall and spaced horizontally from said vertical sidewall of said gate electrode to define a vertical passage having horizontal dimensions appropriate for the synthesis of said semiconducting nanotube, said semiconducting nanotube positioned in said vertical passage, and said spacer extending vertically relative to said gate electrode such that said vertical passage has a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode; a gate dielectric disposed on said vertical sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube. Dependent claims 2-5 and 8-15 depend either directly or indirectly from claim 1. Accordingly, each of dependent claims 2-5 and 8-15 is believed to be allowable based upon at least the allowability of independent claim 1 and, furthermore, upon other features set forth in dependent claims 2-5 and 8-15 but not discussed herein.

With respect to independent claim 42, the prior art fails to disclose or suggest a semiconductor device structure, comprising: a substrate; a gate electrode projecting from said substrate and including a sidewall; a spacer of a dielectric material flanking said sidewall to define a passage; a semiconducting nanotube positioned in said passage between said sidewall and said spacer and extending between opposite first and second ends; a gate dielectric disposed on said sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source. Dependent claims 43-46 depend either directly or indirectly from claim 42. Accordingly, each of dependent claims 43-46 is believed to be allowable based upon at least the allowability of independent claim 42 and, furthermore, upon other features set forth in dependent claims 43-46 but not discussed herein.

With respect to independent claim 47, the prior art fails to disclose or suggest a semiconductor device structure fabricated on a substrate, the semiconductor device structure comprising: a gate electrode projecting from the substrate and including a sidewall; a spacer of a

dielectric material flanking said sidewall of said gate electrode to define a passage; a semiconducting nanotube positioned in said passage between said sidewall of said gate electrode and said spacer, said semiconducting nanotube extending between opposite first and second ends; a gate dielectric disposed on said sidewall of said gate electrode between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source, and said semiconducting nanotube having a length such that said second end of said semiconducting nanotube projects beyond said gate electrode and into said drain. Dependent claims 48-52 depend either directly or indirectly from claim 47. Accordingly, each of dependent claims 48-52 is believed to be allowable based upon at least the allowability of independent claim 47 and, furthermore, upon other features set forth in dependent claims 48-52 but not discussed herein.

If the Examiner disagrees with any of these comments, he is respectfully requested to provide further explanation on the record. Applicants do not believe that any fees are due in connection with this submission. However, if such petition is due or any fees are necessary, the Commissioner may consider this to be a request for such and charge any necessary fees to deposit account 23-3000.

Respectfully submitted,

January 8, 2007
Date

/William R. Allen/

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